REMARKS

Claims 1-3, 5-9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. (U.S. 5,372,968) in view of Bose et al. (U.S. 5,492,858). Claims 1, 4-5, 8, 10-11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkatesan et al. (U.S. 5,459,096) in view of Bose et al. (U.S. 5,492,858).

1. Correction of drawings:

Figures 1-6 should be designated by a legend such as -Prior Art-because only that which is old is illustrated. See MPEP 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Response:

A legend, Prior Art, has been added in each of Figs.1-6 as shown in the attached drawings. No new matter is introduced. Allowance of the drawing changes is hereby requested.

2. Correction of the specification under 37 CFR 1.121:

A correction of the specification under 37 CFR 1.121 has been provided. Although the correction has significant revisions, it is the belief of the Applicant that no new material has been introduced into the present application.

In general, changes have been made simply to correct grammatical errors. In particular, the peculiar term "a positive photoresist layer 62" in the specification has been replaced by the term "a negative photoresist layer 62". Since a negative photoresist layer becomes dissolved after it is exposed to light beams, the term "a positive photoresist layer 62" has to be changed to the term "a negative photoresist layer 62" for supporting the validity of Fig.12. Additionally, an incorrect item numbers 85, 80, and 90 have been changed to the correct value of 72, 70, and 80 respectively. Support for changing the above-mentioned item numbers can be found in the Figs.13-14. Consideration of the correction is politely requested.

3. Rejection over claims 1-3, 5-9, and 12:

Lur et al. discloses forming a plurality of shallow trenches and generating at least one dummy on the trenches (Fig.1-2, col.3, lines 28-32). Lur et al. teaches forming trenches having different widths and the width of some trenches being greater than others (Fig.2). Lur et al. shows forming a dielectric layer to fill the trenches and planarizing the structure to align the surface of the dielectric layer inside each trench with the surface of each component on the semiconductor wafer (Fig.4-6, col.3, lines 60-65). Lur et al. teaches the dummy being made of silicon and the dummy remaining covered by the dielectric material (Fig.5-6). Lur et al. shows implanting into the substrate through the openings in the mask (col.3, lines 50-55).

Lur et al. teaches forming a pad oxide layer on the substrate, forming a pad nitride layer on the pad oxide layer, and planarizing the structure by a first and a second planarization process (Fig.1-5, col.3, lines 15-30, 64-66, col.4, lines 2-35).

Lur et al. does not specifically show condensing the dielectric layer by using an annealing process, the first planarization process being a polishing process. However, Bose et al. shows forming shallow trenches on a semiconductor substrate using photolithography and etching process (col.4, lines 48-55). Bose et al. teaches filling the trenches employing TEOS and condensing the dielectric layer by using an annealing process (col.5, lines 5-20). In addition, Bose et al. shows chemical mechanical polishing to planarize the surface (col.5, lines 18-25) the width of the trenches being less than 2 microns (col.4, lines 60-61), and performing a second planarization process (col.5, lines 20-25).

Regarding the specific width and height as claimed, the selection of any appropriated variable for a known process is within the capabilities of a person of ordinary skill in the art.

Since Lur et al. and Bose et al. are both from the same field of endeavor of forming trenches; the purpose disclosed by Lur et al. would have been recognized in the pertinent of Bose et al.

Therefore, it would have been obvious to a person

of ordinary skill in the art at the time of the invention to modify Lur et al. reference by including the teaching of Bose et al. in order to increase the etch resistant of the dielectric layer and to avoid recessing of the dielectric layer (Bose et al., col.4, lines 4-8).

Response:

First, claim 1 is amended according to the specification of page 5, lines 12-30, and page 6, lines 1-19. No new matter is introduced.

Second, the Applicants intend to point out the difference between the amended claim 1 of the present application and the Lur et al.'s disclosure in view of Bose et al.'s teaching. The amended claim 1 of the present application is repeated below:

"1. A method for electrically isolating shallow trenches between components on the surface of a semiconductor wafer comprising:

(a) forming a plurality of first-type trenches and second-type trenches on a semiconductor substrate, each of the first-type trenches having a width greater than a predetermined size that is greater than a width of each of the second-type trenches;

(b) performing a photolithographic process to form at least one photoresist pattern in each of the first-type trenches;

(c) performing an etching process to form at least one dummy and a plurality of third-type trenches in each of the first-type trenches with the

photoresist patterns as masks, and to deepen each of the second-type trenches;

(d) stripping the photoresist patterns;

(e) forming a dielectric layer over the surface of the semiconductor wafer, wherein the dielectric material of the dielectric layer fills the first-type trenches, the second-type trenches, and the third-type trenches on the surface of the semiconductor wafer;

(f) condensing the dielectric layer; and

(g) performing a planarization process to polish the surface of the semiconductor wafer for aligning the surface of the dielectric layer inside each of the first-type trenches and the second-type trenches with the surface of each component on the semiconductor wafer."

As described in the amended claim 1, a photolithographic process is performed to form the photoresist patterns 40 on the Si substrate 34, and then, the surface of the Si substrate 34 not covered by photoresist patterns 40 is etched to form the dummies 48 and the trenches 42 (page 6, lines 5-19, and Fig.9-11). Accordingly, **the present invention utilizes the photoresist patterns 40 as masks while the Si substrate 34 is etched to form the dummies 48 and the trenches 42. In addition, a plurality of dummies 48 can be simultaneously formed within the trench 46 in the present application** (Fig.11).

However, neither Lur et al. nor Bose et al. teach to form the dummies and the trenches through utilizing

the photoresist patterns as masks. Lur et al. disclose that a pair of silicon nitride spacers 16 is formed on the sidewalls of the silicon dioxide layer 12, and a spin-on-glass layer 18 is formed within the wide opening 15 (Fig.1 and col.3, lines 24-41). Additionally, Lur et al. further teach that the silicon nitride spacers 16 are removed and deep trenches 19 are etched into the silicon substrate under the silicon nitride spacers. Thus, **Lur et al. utilizes the spin-on-glass layer 18 as a mask while the silicon substrate 10 is etched to form the dummy and the deep trenches 19. Furthermore, only one dummy can be formed once within the wide opening 15 in Lur et al.'s disclosure, but a plurality of dummies can be simultaneously formed within the trench 46 in the present application.** It is therefore believed that the methods disclosed in the present application should be different from Lur et al.'s disclosure.

Moreover, Bose et al. teach a method of planarizing a surface of a semiconductor substrate (Fig.4-5, col.5, lines 41-67, and col.6, lines 1-3). Bose et al. never disclose to form a plurality of dummies and trenches within a large trench. Accordingly, the method disclosed in the present application is quite different from that disclosed in Bose et al.'s disclosure.

Form the above discussion, since neither Lur et al. nor Bose et al. suggest utilizing a plurality of photoresist patterns as masks while the Si substrate is etched to form a plurality of dummies and trenches as is suggested in the present application, it is believed non-obvious to one of ordinary skill in the

art at the time the invention was made to combine Lur et al. and Bose et al.'s disclosures to form the art disclosed in the amended claim 1. Reconsideration of the amended claim 1 is hereby requested.

As claims 2-3, 5-9, and 12 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of the claims 2-3, 5-9, and 12 is hereby requested.

4. Rejection over claims 1, 4-5, 8, 10-11, and 13:

Venkatesan et al. discloses forming a plurality of shallow trenches and generating at least one dummy on the trenches (col.5, lines 5-15). Venkatesan et al. teaches forming trenches having different widths and the width of some trenches being greater than others (Fig.2). Venkatesan et al. shows forming a dielectric layer (TEOS) to fill the trenches (col.5, lines 30-35). Venkatesan et al. discloses chemical mechanical polishing to planarize the surface in order to be aligned with the components (Fig.6). Venkatesan et al. shows forming shallow trenches on a semiconductor substrate using photolithography and etching process (col.5, lines 5-15). Venkatesan et al. showns performing a second planarization process to strip off (etching) the pad oxide layer and pad nitride layer from the surface (Fig.7, col.6, lines 40-45).

Venkatesan et al. does not specifically show condensing the dielectric layer by using an annealing process. However, Bose et al. shows condensing the dielectric layer by using an annealing process as

conventional in the art (col.4, lines 4-10, col.5, lines 14-15).

Since Venkatesan et al. and Bose et al. are both from the same field of endeavor of forming trenches; the purpose disclosed by Bose et al. would have been recognized in the pertinent art of Venkatesan et al.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Venkatesan et al. reference by including the teaching of Bose et al. in order to increase the etch resistant of the dielectric layer and to avoid recessing of the dielectric layer (Bose et al., col.4, lines 4-8).

Response:

As described in the amended claim 1, a plurality of first-type trenches and second-type trenches are firstly formed on a Si substrate 34 (Fig.8, and page 6, lines 1-4). Then, a photolithographic process is performed to form the photoresist patterns 40 on the Si substrate 34, and then, the surface of the Si substrate 34 not covered by photoresist patterns40 is etched to form the dummies 48 and the trenches 42 (page 6, lines 5-19, and Fig.9-11). That is, **the present application teaches to form a plurality of dummies 48 and trenches 42 within the shallow trench 46 for reducing a dishing issue.** Additionally, **as shown in Fig.11, a top surface of each dummy 48 is located <u>below</u> a surface of the Si substrate 34.**

However, in the prior art disclosed by Venkatesan

et al., the isolation regions 16 and a region between the isolation regions 16 are formed concurrently, and **a top surface of the region between the isolation regions 16 is level with a surface of the substrate 10** (Fig.1b, and col.5, lines 5-15). Accordingly, the region between the isolation regions 16 is different from the dummies 48 disclosed in the present application. Additionally, Venkatesan et al. disclose a method for forming a planarizied surface in a semiconductor device (Fig.2-7), but Venkatesan et al. never suggest forming a plurality of dummies and trenches within a shallow trench for reducing a dishing issue. Accordingly, it is believed that the methods disclosed in the present application should be different from Venkatesan et al.'s disclosure.

Moreover, Bose et al. teach a method of planarizing a surface of a semiconductor substrate (Fig.4-5, col.5, lines 41-67, and col.6, lines 1-3), but Bose et al. never disclose to form a plurality of dummies and trenches within a shallow trench for reducing a dishing issue. Accordingly, the method disclosed in the present application is quite different from that disclosed in Bose et al.'s disclosure.

Form the above discussion, since neither Venkatesan et al. nor Bose et al. suggest forming a plurality of dummies and trenches within a shallow trench for reducing a dishing issue as is suggested in the present application, it is believed non-obvious to one of ordinary skill in the art at the time the invention was made to combine Venkatesan et al. and Bose et al.'s

disclosures to form the art disclosed in the amended claim 1. Reconsideration of the amended claim 1 is hereby requested.

As claims 4-5, 8, 10-11, and 13 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of the claims 4-5, 8, 10-11, and 13 is hereby requested.

5. Introduction of the new claims 14-18:

The new claim 14 is introduced according to Figs.12-17 and the specification of pages 6-9 of the present application. No new matter is introduced. Allowance of the new claim 14 is respectfully requested.

Additionally, the new claims 15-18 are dependent on the new claim 14 and should be allowed if the new claim 14 is allowed. Allowance of the new claims 15-18 is hereby requested.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

1. On page 6, lines 20-31, and page 7, lines 1-15, please replace the paragraph with the following:

Also, because of different degrees of exposure (the areas on the optical mask with different light penetration capability), a plurality of dummies <u>is</u> [are] generated at the bottom of the chosen shallow trenches at the time the shallow trenches are first formed. Please refer to Fig.12. Fig.12 shows the second method of forming dummies according to the present invention. In this scheme, one mask photo is used to place an optical mask 60 above the semiconductor wafer 30 and to expose and transfer patterns by using different light penetration capability on the optical mask 60. The surface of the semiconductor wafer 30 comprises a Si substrate 34, a pad oxide layer 36, a pad nitride layer 38 and a [positive] <u>negative</u> photoresist layer 62. The optical mask 60 comprises a plurality of areas (the space parts) of which the light penetration capability is 100%, a plurality of areas (the parts with oblique lines) of which the light penetration capability is 0% and a plurality of areas (the parts with horizontal lines) of which the light penetration capability is between 0% to 100%; therefore, the corresponding photoresists 64 are either completely dissolved, not dissolved at all or partly dissolved on the [positive] <u>negative</u> photoresist layer 62 of semiconductor wafer 30 and used as masks. Thus, after etching is repeated,

the semiconductor wafer 30 with a plurality of dummies and shallow trenches, as shown in Fig.11, is made.

2. On page 7, lines 16-31, and page 8, lines 1-9, please replace the paragraph with the following:

Please refer to Fig.13 and Fig.14. Fig.13 and Fig.14 show the third method of forming dummies according to the present invention and is similar with the second method shown in Fig.12. In the third method, a plurality of photoresists 72 is generated by exposing with different degrees of decomposition on the semiconductor wafer 30 twice. Three groups of photoresists 72, completely dissolved, undissolved and partly dissolved, are formed on the surface of semiconductor wafer 30 and are used as masks when etching. As shown in Fig.13, the method requires being exposed twice. First, a plurality of undissolved photoresists [85] 72 are applied to the surface of semiconductor wafer 30 by using an optical mask [80] 70 with areas with light penetration capability of 100% (the space parts) and areas with light penetration capability of 0 % (the parts with oblique lines). Next, the photoresists 74 that determine the positions of dummies and new shallow trenches are partly dissolved by using another optical mask [90] 80 (as shown Fig.14) comprising both areas with light penetration capability of 100% (the space parts) and 0% (the parts with oblique lines). After etching, the semiconductor wafer 30 with a plurality of dummies and shallow trenches as shown in Fig.11 is made.

In the claims:

1. (Once amended) A method for electrically isolating shallow trenches between components on the surface of a semiconductor wafer comprising:

(a) forming a plurality of first-type trenches and second-type trenches on a semiconductor substrate, each of the first-type trenches having a width greater than a predetermined size that is greater than a width of each of the second-type trenches;

(b) [choosing shallow trenches with widths greater than a predetermined size on the surface of the semiconductor wafer and generating] performing a photolithographic process to form at least one [dummy] photoresist pattern in each of the first-type [chosen shallow] trenches [to form a plurality of shallow trenches with widths less than the predetermined size];

(c) performing an etching process to form at least one dummy and a plurality of third-type trenches in each of the first-type trenches with the photoresist patterns as masks, and to deepen each of the second-type trenches;

(d) stripping the photoresist patterns;

(e) forming a dielectric layer over the surface of the semiconductor wafer, wherein the dielectric material of the dielectric layer fills the first-type trenches, the second-type trenches, and the third-type trenches [each shallow trench] on the surface of the semiconductor wafer;

(f) condensing the dielectric layer; and

(g) performing a planarization process to polish the surface of the semiconductor wafer for aligning the surface of the dielectric layer inside each of the first-type trenches and the second-type trenches [shallow trench] with the surface of each component on the semiconductor wafer.

2. (Once amended) The shallow trench isolation method of claim 1 wherein the predetermined size [for the chosen shallow trenches] is about 2 μm.

5. (Once amended) The shallow trench isolation method of claim 1 wherein each component on the semiconductor wafer surface comprises a Si substrate, a pad oxide layer above the Si substrate, and a pad nitride layer above the pad oxide layer, and the planarization process performed on the dielectric layer surface makes this surface inside each of the first-type trenches and the second-type trenches [shallow trench] align approximately with the pad nitride layer of each component on the semiconductor wafer surface; wherein the shallow trench isolation method further comprises:

performing a second planarization process to strip off the pad oxide layer and pad nitride layer from each component, and make the surface of the dielectric layer inside each of the first-type trenches and the second-type trenches [shallow trench] approximately align with the surface of the Si substrate of each component.

6. (Once amended) The shallow trench isolation method

of claim 5 wherein the bottom of each of the first-type trenches and the second-type trenches [shallow trench] on the semiconductor wafer is formed by a Si substrate, and each dummy [formed in each chosen shallow trench] is also made of Si.

7. (Once amended) The shallow trench isolation method of claim 6 wherein after the second planarization process, the dielectric material formed in each of the first-type trenches [chosen shallow trench] remains covered over each Si dummy for electrical isolation.

12. (Once amended) The shallow trench isolation method of claim 1 wherein [the dummy within each chosen shallow trench is generated by using a photolithography and etching process, and] each dummy is formed at the bottom of each of the first-type trenches [shallow trench].

13. (Canceled)

14. (New) A method for forming electrically isolating shallow trenches between components on the surface of a semiconductor wafer comprising:

(a) providing a semiconductor substrate having at least a firs-type trench region used to form a first-type trench, and a second-type trench region used to form a second-type trench, the first-type trench having a width greater than a predetermined value that is greater than a width of the second-type trench;

(b) forming a first photoresist pattern on the semiconductor substrate exposing the first-type

trench region and the second-type trench region, and at least a second photoresist pattern on the first-type trench region, the second photoresist pattern having a smaller height than the first photoresist pattern;

(c) etching the first-type trench region and the second-type trench region to form the first-type trench and the second-type trench with the first photoresist pattern as a mask, and to form at least one dummy at a bottom of the first-type trench with the second photoresist pattern as a mask;

(d) stripping the first photoresist pattern and the second photoresist pattern;

(e) forming a dielectric layer over the surface of the semiconductor substrate, wherein the dielectric material of the dielectric layer fills the first-type trench and the second-type trench on the surface of the semiconductor substrate;

(f) condensing the dielectric layer; and

(g) performing a planarization process to polish the surface of the semiconductor wafer for aligning the surface of the dielectric layer inside each of the first-type trench and the second-type trench with the surface of each component on the semiconductor substrate.

15. (New) The method of claim 14 further comprising:

forming a photoresist layer over the semiconductor wafer; and

utilizing an optical mask of different sets of

light penetration capability to perform a photolithography process on the photoresist layer for simultaneously forming the first photorsist pattern and the second photoresist pattern in the photoresist layer.

16. (New) The method of claim 14 further comprising:

forming a photoresist layer over the semiconductor wafer;

exposing the photoresist layer to light through a first optical mask of different sets of light penetration capability to define the first photorsist pattern;

exposing the photoresist layer to light through a second optical mask of different sets of light penetration capability to define the second photoresist pattern; and

developing the photoresist layer to form the first photorsist pattern and the second pattern.

17. (New) The method of claim 14 wherein the predetermined value is about 2 μm.

18. (New) The method of claim 14 wherein a preferred height of any dummy is around 300 Å to 500 Å.

Sincerely yours,

Winston Hsu Date: 7/4/2003

Winston Hsu, Patent Agent No.41,526

P.O. BOX 506
Merrifield, VA 22116
U.S.A.
e-mail:winstonhsu@naipo.com.tw

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